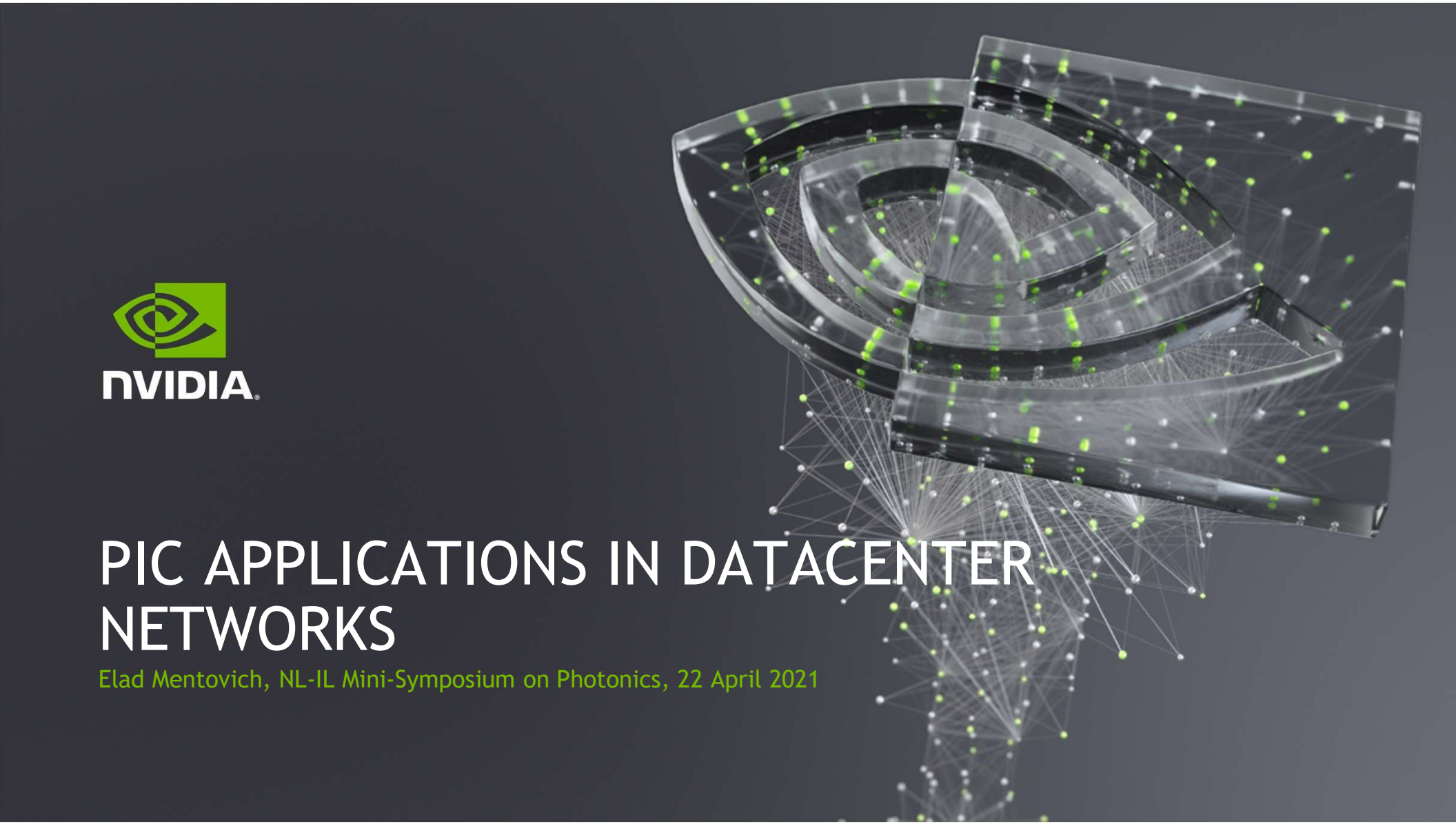


PIC APPLICATIONS IN DATACENTER NETWORKS

Elad Mentovich, NL-IL Mini-Symposium on Photonics, 22 April 2021

NVIDIA AT A GLANCE

Accelerated Computing Pioneer

Brief History

1993: Founded by Jensen Huang, Chris Malachowsky, and Curtis Priem

1999: IPO on NASDAQ at $12 (prior to 4 stock splits, now 12:1)

2001: Xbox win; fastest semiconductor company to reach $1B in sales

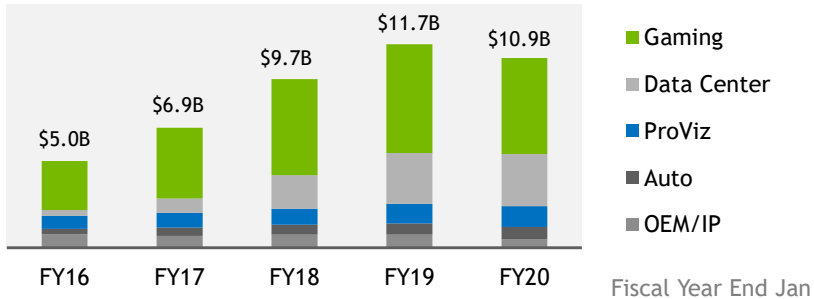
2006: Unveils CUDA architecture, expanding to scientific computing

2009: Inaugural GPU Technology Conference (GTC)

2016: Introduces first products for AI and autonomous driving

2020: NVIDIA acquires Mellanox to become a leader in Data Center Networking

Revenue by Market Platform



Recognitions

Harvard Business Review's **The CEO 100**

Fortune's **Best Places to Work**

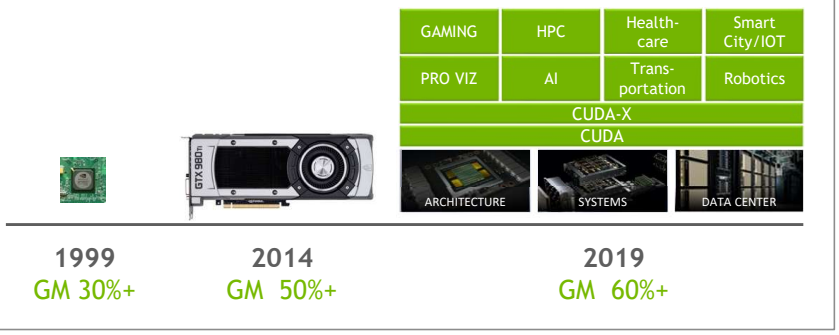
MIT Tech Review's **50 Smartest Companies**

Fortune's **World's Most Admired Companies**

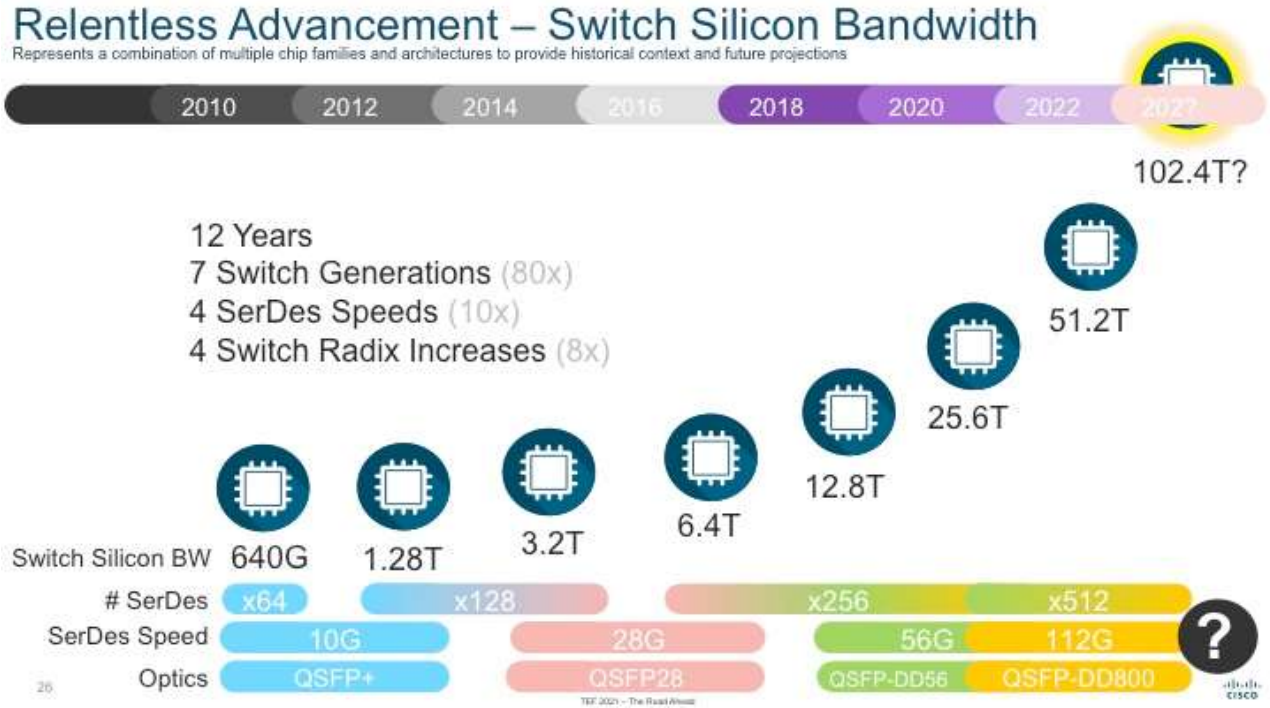
Forbes **JUST 100 Best Corporate Citizens**

Dow Jones **Sustainability Index**

From Chip Vendor to Computing Platform



DATACENTER SCALING TRENDS

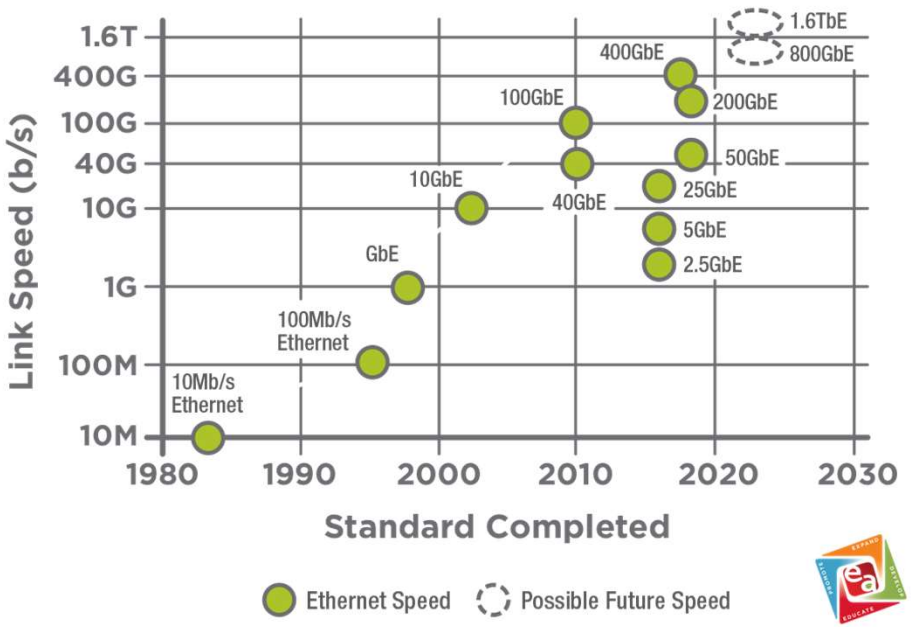


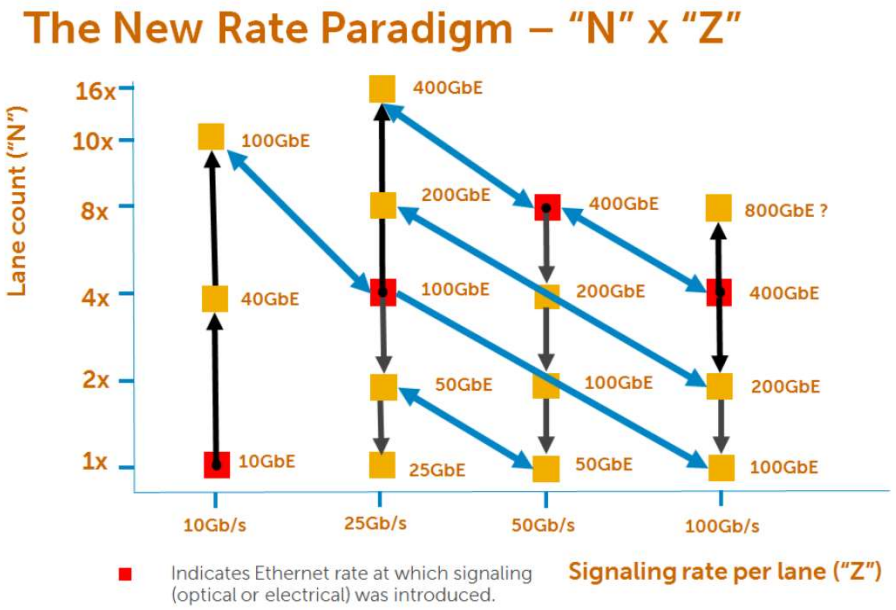
Source: Rakesh Chopra, Cisco Systems @ TEF 2021

- Switch scale-up and scale-out
- 100G SerDes enables 800G transceivers
- 200G SerDes will enable 1.6 Tb/s

WHAT IS COMING AFTER 400G?

Interconnect speed evolution





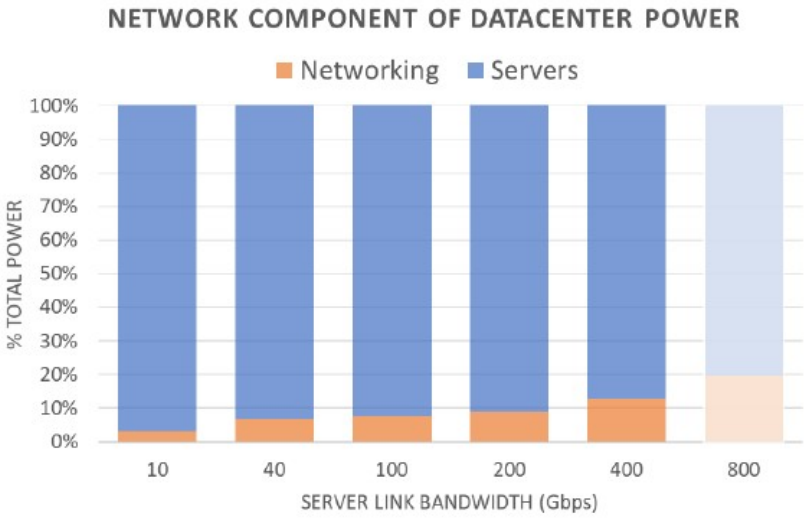
Source: John D' Ambrosia

- Diverging speeds for diverging customer needs
- Next speed range from 800 Gb/s – 1.6 Tb/s
- Rate paradigm has worked well in last generations

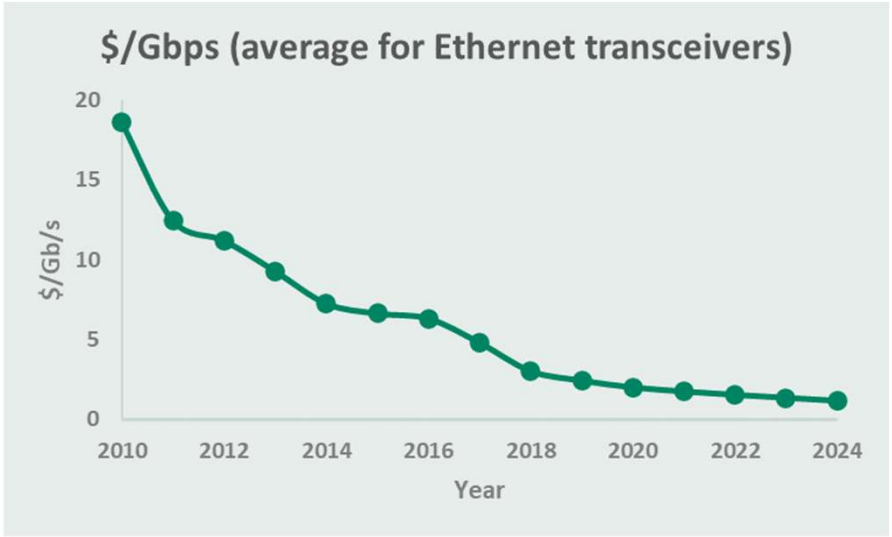
NVIDIA

SCALING CHALLENGES

Power, cost



Source: MIcrosoft



- Network power is taking up valuable system resources
- New solutions need to reach (at least) parity in cost/bit
- 400G flexibility still needed (diversity in medium interfaces, reaches)
- Can we continue to apply the scaling paradigm?

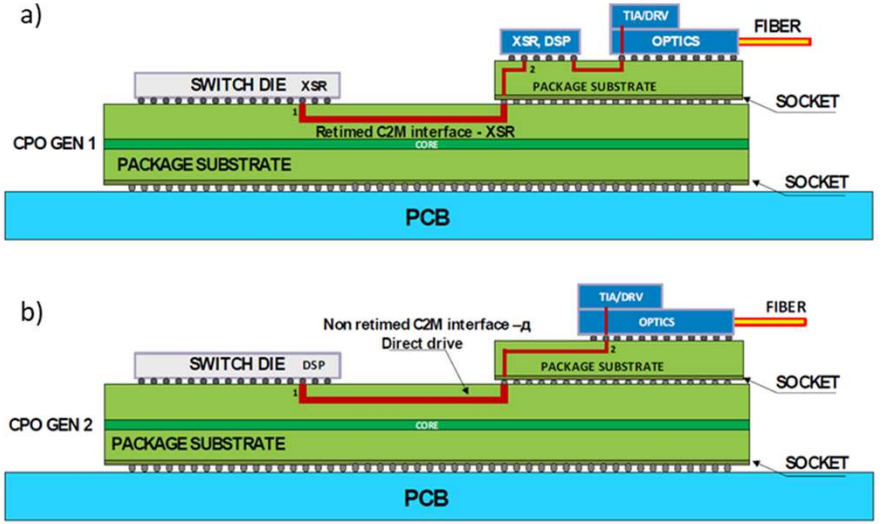
PHOTONIC INTEGRATION TO THE RESCUE

Large scale photonic integration can **add transceiver value**

- Increase bandwidth density
- Reduce cost/bit for many optical lanes
- Scale speed by miniaturization & close electronics integration
- ++ value beyond current conventional optics

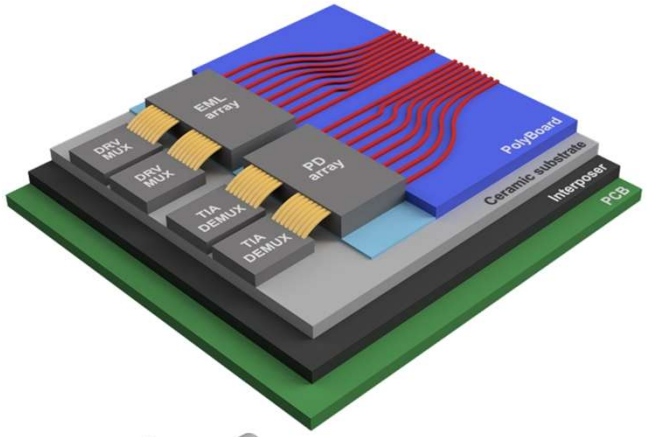
What integration platform?

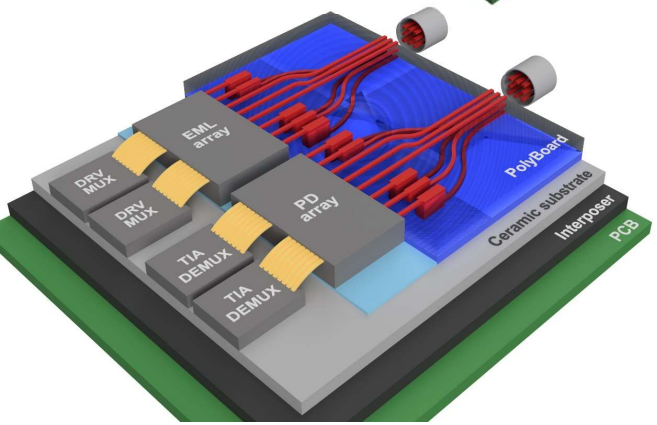
- no one-size-fits-all
- different requirements for diverging customer needs
- adopting fabless model



H2020 PROJECT POETICS

CoPackaging of Terabit direct-detection and coherent Optical Engines and switching circuits in mulTI-Chip moduleS for Datacenter networks and the 5G optical fronthaul





- Elevated temperature EMLs
- PolyBoard polymer waveguide platform
- Interface to MCF
- 200 Gb/s PAM4
- 100 Gbaud analog mux/demux
- 1.6 Tb/s prototype platform

POETICS

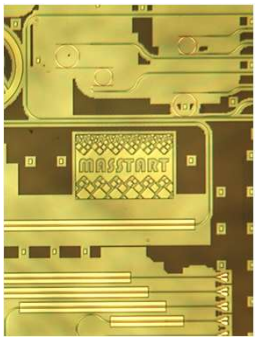
ict-poetics.eu

ICCS · LIONIX INTERNATIONAL · Optagon Photonics · Mellanox TECHNOLOGIES · Fraunhofer Heinrich-Hertz-Institut · imec · phix · TIM

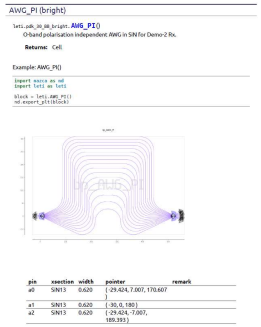
NVIDIA

H2020 PROJECT MASSTART

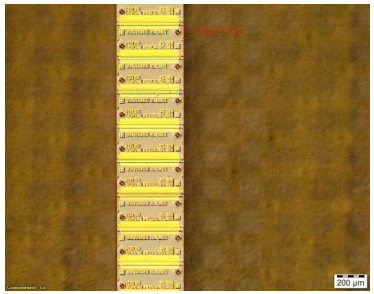
MASS manufacturing of TrAnsceiveRs for Terabit/s era



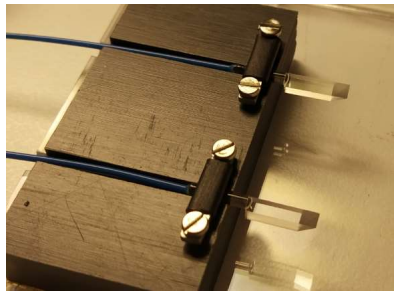
CEA-Leti 50 Gbaud Silicon Photonics



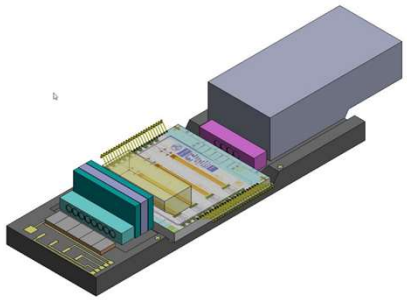
Bright Design Kit



ALMAE laser arrays

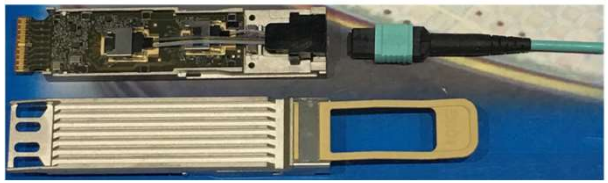


TEEM WAFT



DUST silicon bench

FICONTEC & Tektronix automation



NVIDIA Networking integration

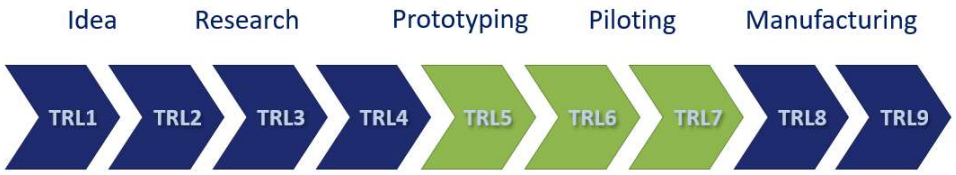
MASSTART

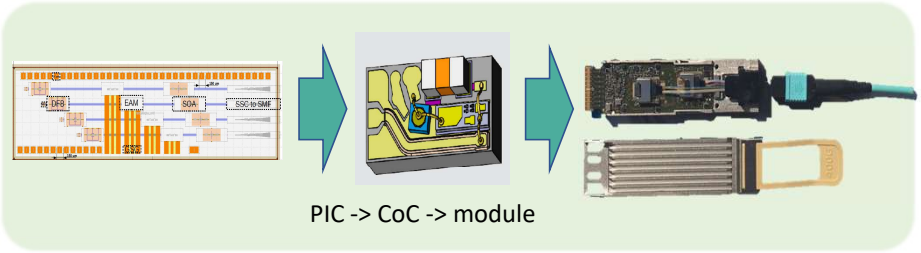
masstart.eu/

NVIDIA

H2020 PROJECT INPULSE: THE JEPPIX PILOT LINE

From prototype to pilot production





1. Create manufacturing process design kits by using smart testing to efficiently collect manufacturing statistics
2. Increase capacity for open access industrial prototyping and systematically improve performance of the building blocks
3. Validate the pilot line with two experienced participants to validate and stretch the platform performance beyond state-of-the-art
4. Demonstration through tens of external user designs
5. Establish a sustainable business model with a resilient industrial ecosystem to ensure continued open-access after four years
6. Support businesses as they scale to volume production

JEPPIX

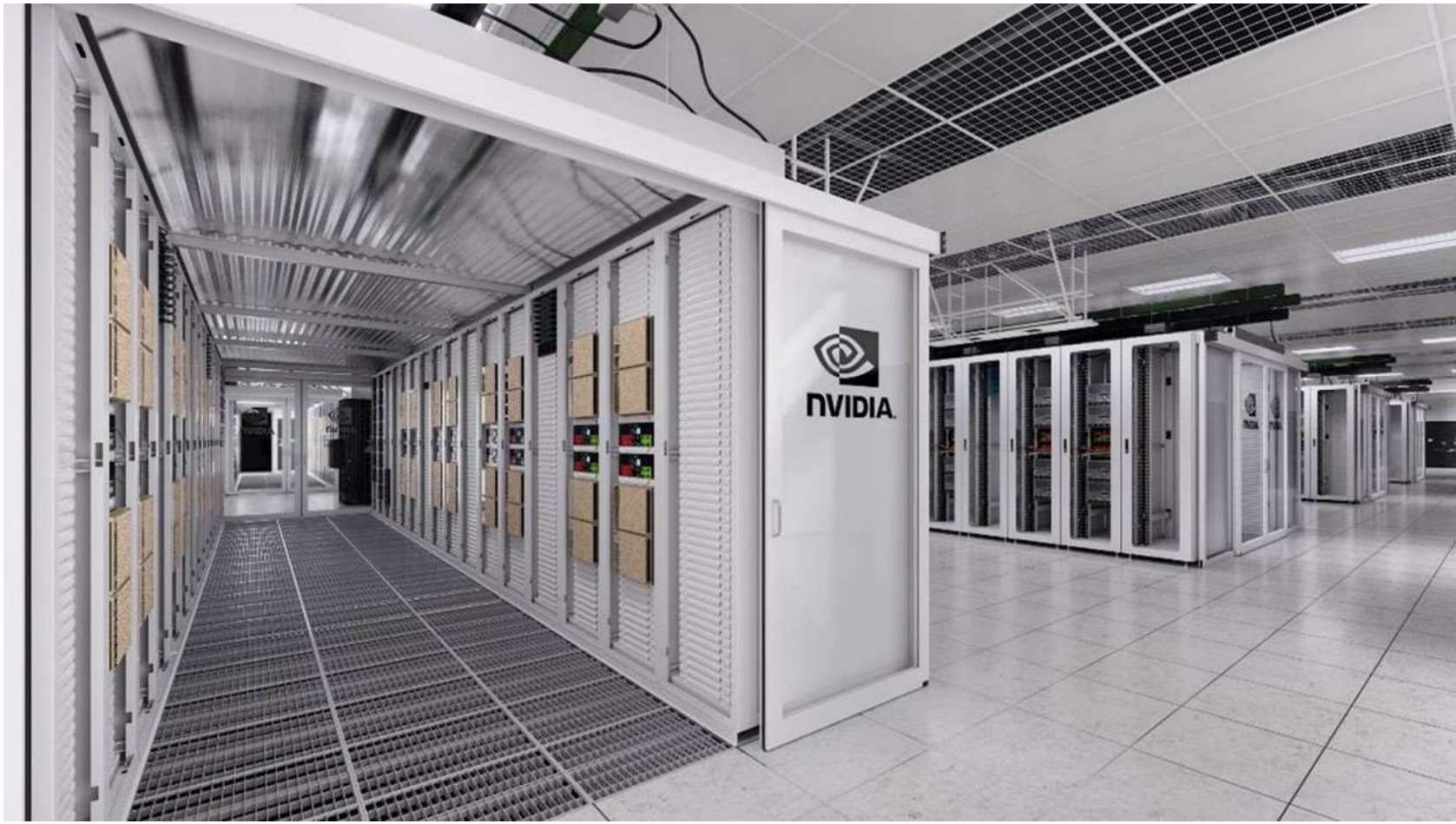
pilotline.jeppix.eu/

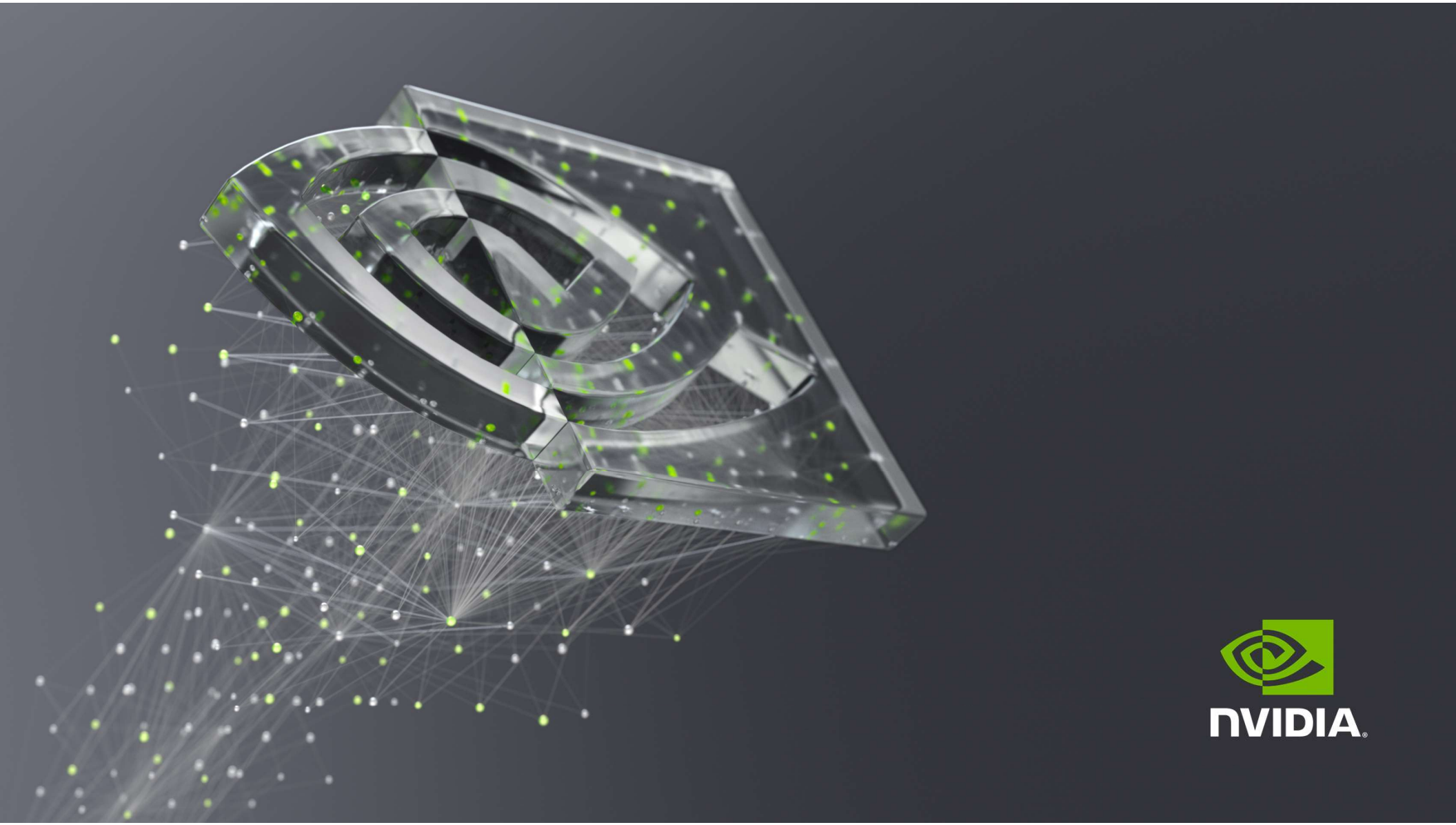
NVIDIA

THANK YOU

Elad Mentovich

mentovich@nvidia.com




NVIDIA